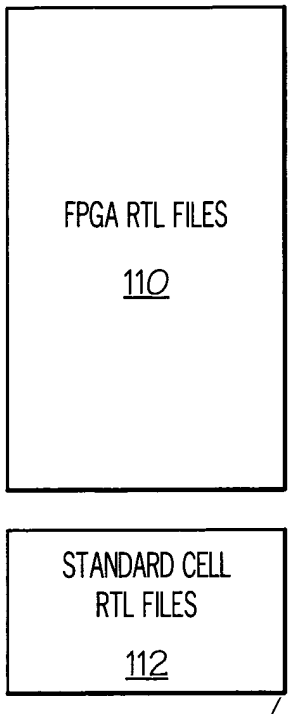


FIG. 1A
(PRIOR ART)

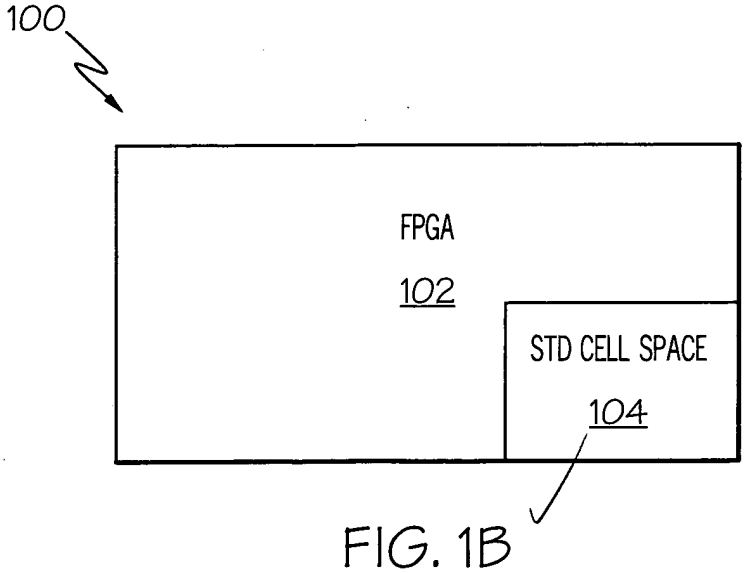


FIG. 1B

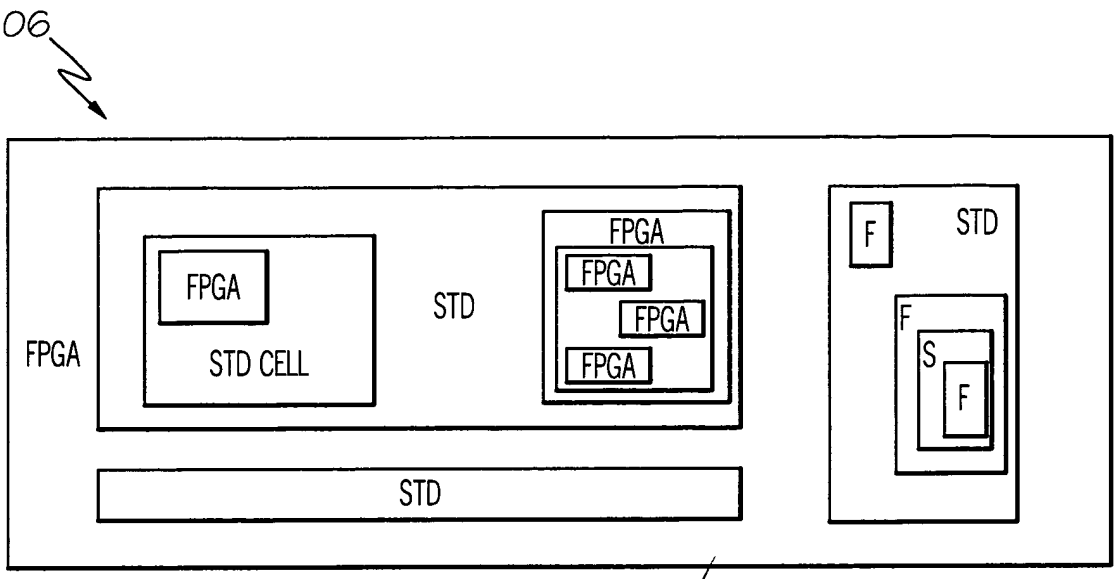


FIG. 1C

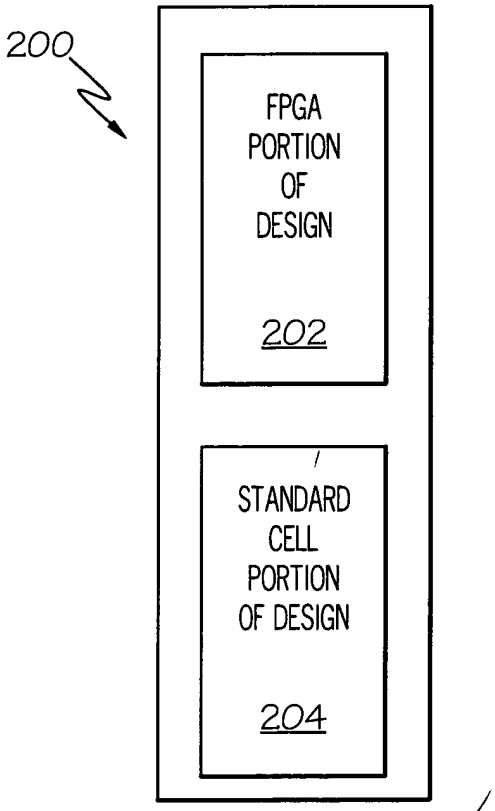
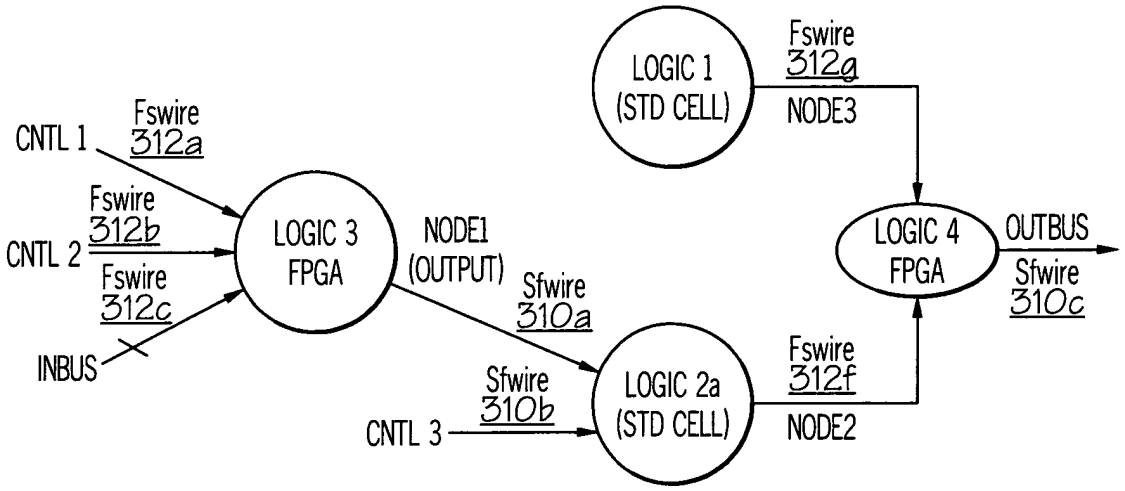


FIG. 2

	WIRE TYPE	MEANING	FIXED OR ADJUSTABLE
302	(S)wire	STANDARD CEL	FIXED
304	Fwire	FPGA	FIXED
306	sFwire	TOOL REPARTITION REQUEST: FPGA -> STD CELL	ADJUSTABLE
308	fSwire	TOOL REPARTITION REQUEST: STD CELL -> FPGA	ADJUSTABLE
310	Sfwire	STANDARD CELL, ACCEPTED BY DESIGNER	ADJUSTABLE
312	Fswire	FPGA, ACCEPTED BY DESIGNER	ADJUSTABLE

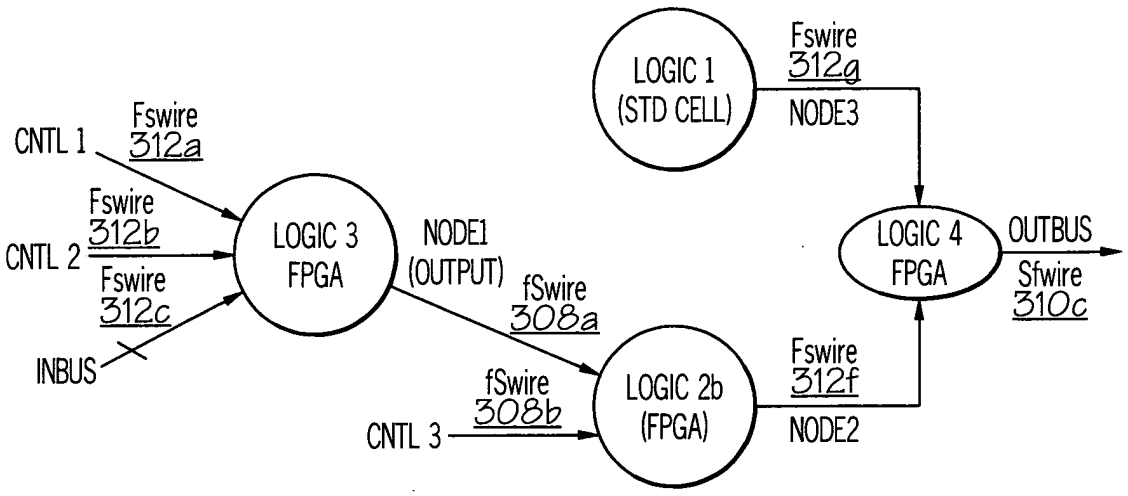
FIG. 3



EXAMPLE VERILOG

```
module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7.0] INBUS;
input Fswire CNTL3;
Sfwire NODE1;
Fswire NODE2, NODE3;
ouput Sfwire [7:0] OUTBUS;
```

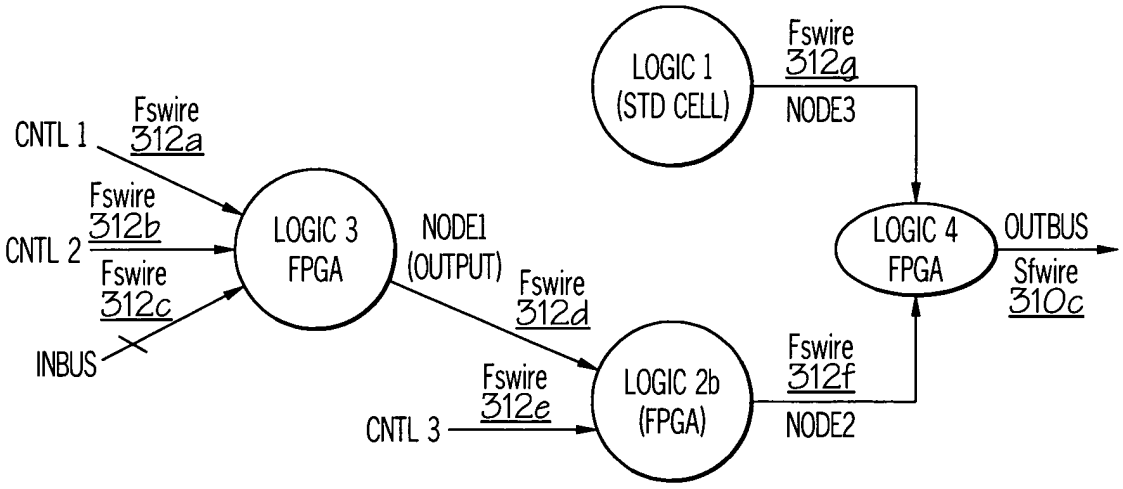
FIG. 4A



EXAMPLE VERILOG

```
module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input Fswire CNTL3;
fSwire NODE1;
Fswire NODE2, NODE3;
ouput Sfwire [7:0] OUTBUS;
```

FIG. 4B



EXAMPLE VERILOG

```
module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7.0] INBUS;
input Fswire CNTL3;
Fswire NODE1;
Fswire NODE2, NODE3;
ouput Sfwire [7:0] OUTBUS;
```

FIG. 4C

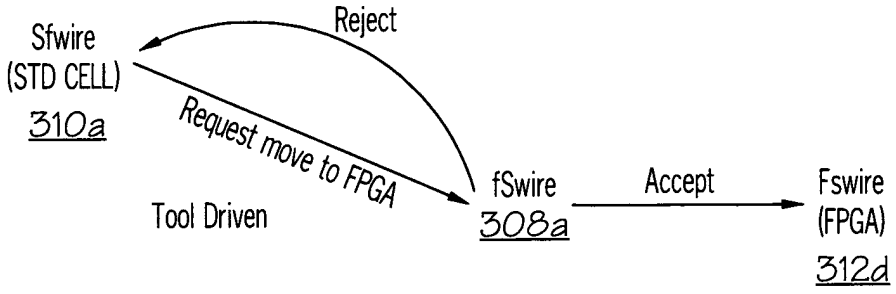

Sfwire
(STD CELL)
310a
Reject
Request move to FPGA
Tool Driven
fSwire
308a
Accept
Fswire
(FPGA)
312d

FIG. 5A

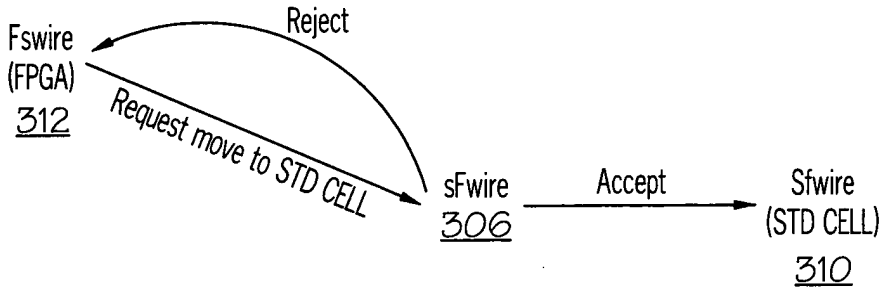

Fswire
(FPGA)
312
Reject
Request move to STD CELL
sFwire
306
Accept
Sfwire
(STD CELL)
310

FIG. 5B

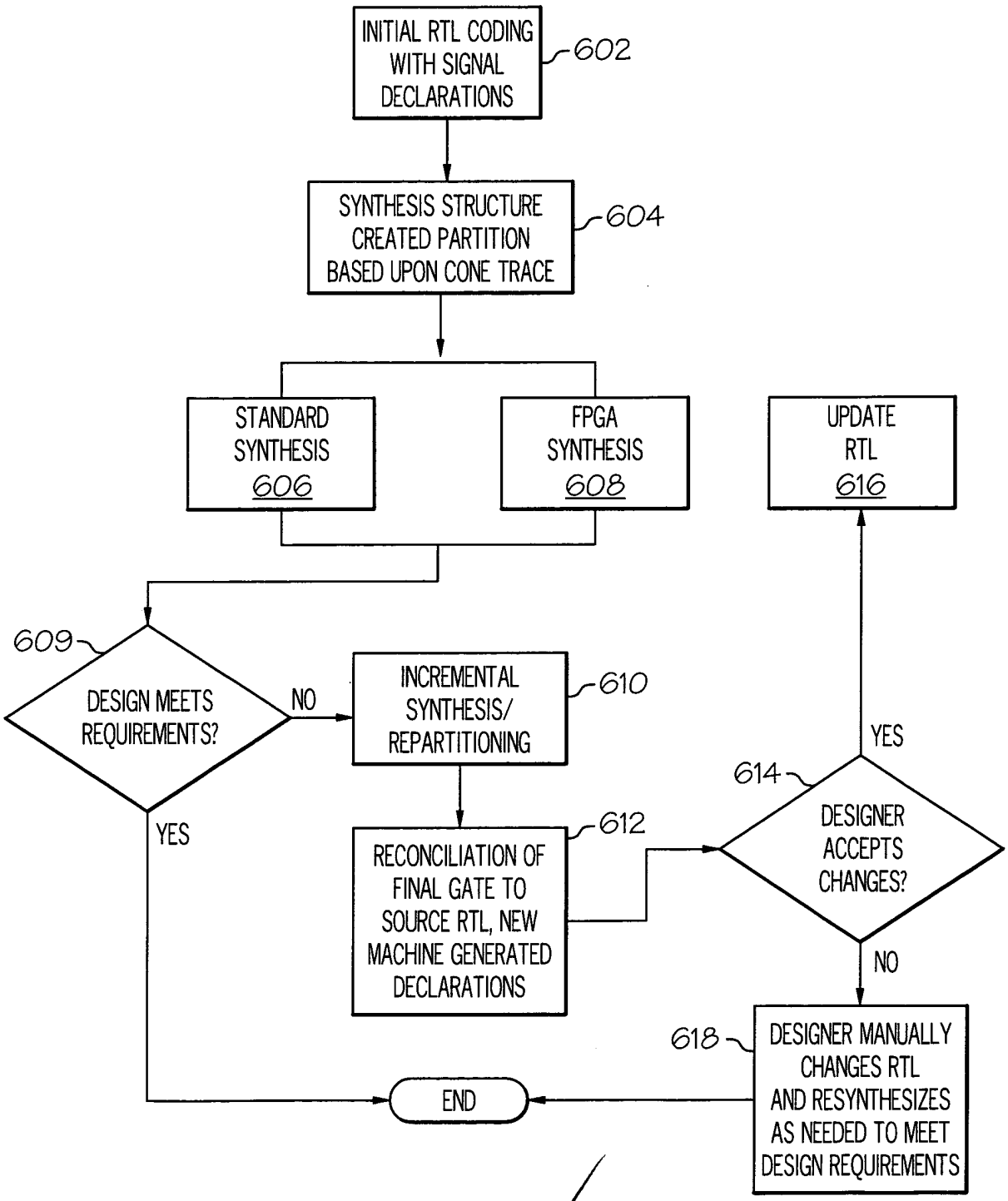

INITIAL RTL CODING WITH SIGNAL DECLARATIONS
602
SYNTHESIS STRUCTURE CREATED PARTITION BASED UPON CONE TRACE
604
STANDARD SYNTHESIS
606
FPGA SYNTHESIS
608
UPDATE RTL
616
609
DESIGN MEETS REQUIREMENTS?
NO
INCREMENTAL SYNTHESIS/ REPARTITIONING
610
YES
RECONCILIATION OF FINAL GATE TO SOURCE RTL, NEW MACHINE GENERATED DECLARATIONS
612
614
DESIGNER ACCEPTS CHANGES?
YES
NO
618
DESIGNER MANUALLY CHANGES RTL AND RESYNTHESIZES AS NEEDED TO MEET DESIGN REQUIREMENTS
END

FIG. 6

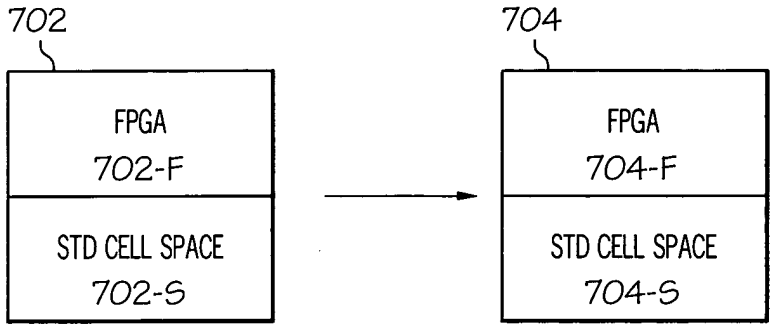

702
FPGA
702-F
STD CELL SPACE
702-S
704
FPGA
704-F
STD CELL SPACE
704-S

FIG. 7A

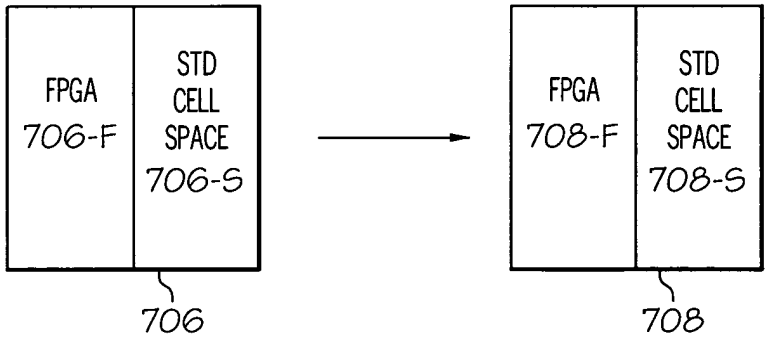

FPGA
706-F
STD
CELL
SPACE
706-S
706
FPGA
708-F
STD
CELL
SPACE
708-S
708

FIG. 7B